DEC STD 030-7
MODULE MANUFACTURING STANDARD — BACKPLANE RULES AND RELATED FACTORS

DOCUMENT IDENTIFIER: A-DS-EL00030-07-0 Rev E, 17-June-1991

ABSTRACT: This section of DEC STD 030 provides the design rules and related factors regarding the design, assembly, and test of all backplanes. Refer to DEC STD 030-0 through 030-10 for other requirements not covered in this text.

APPLICABILITY: This document is mandatory for designs to be compatible with the standard volume manufacturing process. Site Producibility Engineers are available to provide additional information on specific areas not covered in this standard.

STATUS: APPROVED 17-June-1991; use VTX SMC for current status.

This document is confidential and proprietary and is the property of Digital Equipment Corporation. It is an unpublished work protected under the Federal copyright laws.

© Digital Equipment Corporation. 1986, 1991. All rights reserved.

DEC STD 030-7 MODULE MANUFACTURING STANDARD — BACKPLANE RULES AND RELATED FACTORS

DOCUMENT IDENTIFIER: A-DS-EL00030-07-0 Rev E, 17-June-1991

REVISION HISTORY:	Rev A	30-Jun-1986	
	Rev B	06-Feb-1987	ECO Number LJ001
	Rev C	20-May-1988	ECO Number CT002
	Rev D	30-Nov-1989	ECO Number CTS03
	Rev E	17-June-1991	ECO Number CTS04

Document Management Category:	Board, Module, and Backplane (HPB)
Responsible Department:	New Products Producibility
Responsible Person:	Jim Keenan

APPROVAL: This document has been reviewed and recommended for approval by the DEC STD 030 Advisory Committee and the General Review Group for its category.

Jim Keenan, Standard Owner

Eric Williams, Standards Process Manager

Direct requests for further information to:

Jim Keenan

KAO1/8, DTN: 621-2633, POLAR::KEENAN

Use VTX SMC to order copies of this document from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

CONTENTS

1 INTRODUCTION 1
1.1 DEFINITIONS 1
1.2 TYPES OF BACKPLANES 1
1.3 MANUFACTURING TECHNOLOGIES 2
1.4 BACKPLANE PRODUCIBILITY 2

2 COMMON DESIGN RULES FOR BACKPLANES 2

3 COMMON ASSEMBLY RULES FOR BACKPLANES 4

4 TEST RULES FOR BACKPLANES 5

5 WIREWRAP RULES FOR BACKPLANES 7

6 SPECIFIC RULES FOR WAVE-SOLDERED BACKPLANES 8

7 SPECIFIC RULES FOR PRESS-PIN BACKPLANES 10

8 SPECIFIC DESIGN AND ASSEMBLY RULES FOR BACKPLANES WITH SURFACE-CONTACT CONNECTORS 12

9 SPECIFIC DESIGN RULES FOR BACKPLANES WITH SURFACE MOUNT COMPONENTS 12

REFERENCED DOCUMENTS 13

DEC STD 030-7 RULES INDEX 15

INDEX

EXHIBITS

1 Available Standard Hex Module Castings 4
2 Standard Design Data for Mounting Bars 4
3 Maximum Wirewrap Area 7

1 INTRODUCTION

This section of DEC STD 030 specifies design rules for backplanes. Backplane designs must also conform to other applicable rules referenced in this standard. Refer to DEC STD 030-4, Exhibit 2, for required marking features.

1.1 DEFINITIONS

A backplane is an interconnection device for modules. It typically consists of a backpanel, a connector technology (for example, soldered, press-pin or surface-contact connectors), and supporting hardware. Some wiring may be required to achieve all interconnections.

Backpanels are printed-wiring boards, either single-sided, double-sided, multilayer, or multisignal layer, that with the connectors, components, and supporting hardware, form a backplane.

- **Single-Sided PC Board** — Pads and conductors only on the solder side (side 2).
- **Double-Sided PTH** — Conductors and pads on both sides of the board, and the holes drilled through the pads are plated to provide continuity from one side to the other.
- **Multilayer** — Three or more layers of copper. Typically, the outside layers are signal connectors and the inner layers are voltage and ground planes.
- **Multisignal Layer (MSL)** — A multilayer board having three or more signal layers.

Typical support hardware such as castings and mounting bars are used to provide structural support for the backplane. See Rule 7070 and Rule 7080 for further information. Refer to *DEC STD 016 Printed-Wiring Board and Module Manufacturing Terminology* for definitions of other module manufacturing terms.

1.2 TYPES OF BACKPLANES

There are four approved methods of backplane connector design.

- Bussed and wired (does not contain a PC board)
- Wave solder
- Press-pin
- Surface contact connectors

There are two approved methods of backplane component design.

- Through Hole
- Surface Mount

All types of backplanes have advantages and disadvantages and care should be exercised in selecting the type that will meet design requirements and result in the lowest possible manufacturing costs.

1.3 MANUFACTURING TECHNOLOGIES

There are two manufacturing technologies.

- **Surface Contact Connectors** — Surface contact connectors, such as zero insertion force (ZIF) or low insertion force (LIF) connectors, make electrical contact with the backplane by being mounted directly on pads on the board surface (as opposed to using plated-through holes). These connectors are held in place by a mechanical hold-down mechanism.
- **Mixed Technology** — Mixed technology designs use two or more of the manufacturing technologies described in Section 1.2. These designs should be avoided if possible because of the additional process steps and lead times required, resulting in greater manufacturing costs. Consult Kanata Engineering for the impact of a specific mixed technology design.

1.4 BACKPLANE PRODUCIBILITY

There are no standard backplane configurations because of the variability of backplane packaging requirements. All board designs for backplanes must be processed through Pre-Design Producibility. Refer to DEC STD 030-1.

Where possible, avoid putting components on both sides of the backpanel. This increases assembly and test fixture costs and increases assembly labor costs.

2 COMMON DESIGN RULES FOR BACKPLANES

RULE 7000: FINISHED BOARD SIZE

The following are the process constraints with regard to backpanel sizes.

- KAO Wave Solder Machine: 16 inches maximum width
- KAO Aqueous Cleaner: 18 inches maximum width
- KAO Press-Pin Machine: 25 x 28 inches
- KAO Test: 18 x 24 inches
- KAO Surface Mount Test: 24 x 24 inches
- KAO Surface Mount Assembly: 16 x 24 inches (16 x 18 inches maximum onsertion window)

Contact Producibility if the proposed design falls outside any of the categories listed above.

RULE 7010: BACKPANEL SHEARING/ROUTING

The 50-level MD must specify that backpanels are to be cut to their finished size at the board shop. See DEC STD 030-4, Rule 4390 for clearance requirements.

RULE 7020: BASE LAMINATE MATERIAL

FR-4 laminates and bonding sheets (pre-preg) are preferred and shall meet the standard thickness requirements per the appropriate A-PS-1400000-GS-0 series of specifications listed in DEC STD 030-2, Exhibit 2. If materials other than FR-4 are required by design, contact Gerald G. Gagnon of Corporate Printed-Wiring Boards (226-2037, BOARDS::GAGNON).

RULE 7030: SOLDERMASK

Soldermask is required on both sides of backpanels that are soldered, with the exception of MSL pads-only boards. Soldermask over bare copper (SMOBC) is suggested for the following reasons.

- It results in approved solderability (no solder bridges) and is the recommended process for high density (fine-line 1, 2, 3, and 4) backplanes.
- Boards with pads only (no etch lines) on external layers do not require soldermask. Backplane boards with conductors on external layers require soldermask whether re-flowed or not.

Refer to DEC STD 030-1, heading 4.2 for further information.

RULE 7040: COPPER INNER LAYER THICKNESS

See DEC STD 030-4, Rule 4260, for the standard copper inner layer thicknesses.

RULE 7050: PREFERRED INNER LAYER CLEARANCE PAD SIZES

See DEC STD 030-4, Exhibit 27 and DEC STD 030-4, Exhibit 28 for the preferred inner layer clearance pad diameters in power or ground planes for plated-through hole sizes up to 0.040 inch. The inner layer clearance for the 0.041-inch press-pin hole is 0.085 inch.

RULE 7060: BACKPANEL NOMENCLATURE

Identification nomenclature is required on all backpanels produced in Kanata. A decision not to use nomenclature on a backpanel must be made by prior agreement with Kanata Producibility. Nomenclature should be applied to the board side(s) where the components are to be installed.

In general, the nomenclature should indicate component locations, orientations, and pin numbering. Corporate Producibility will help work technical issues concerning the layout of artwork. Nomenclature is not required for surface mount components.

Nomenclature shall not interfere with solderability or electrical functionality. To reduce the cost of board manufacturing operations, all nomenclature should be etched in copper. Where this is not possible, screened nomenclature may be applied. See DEC STD 030-4, Exhibit 2 for screened nomenclature requirements.

3 COMMON ASSEMBLY RULES FOR BACKPLANES

The following rules provide the standard assembly rules for backplanes.

RULE 7070: STANDARD CASTINGS

Exhibit 1 lists the standard hex module castings that are available.

Exhibit 1: Available Standard Hex Module Castings

Casting Size	Part Number
4–Slot (No Standoff)	12–09583–01
4–Slot (With Standoff)	12–09583–00
8–Slot (Quad)	74–13933–00
9–Slot	12–11439–01
14–Slot	74–22423–01

RULE 7080: MOUNTING BARS AND BACKPLANE-TO-EQUIPMENT CONFIGURATIONS

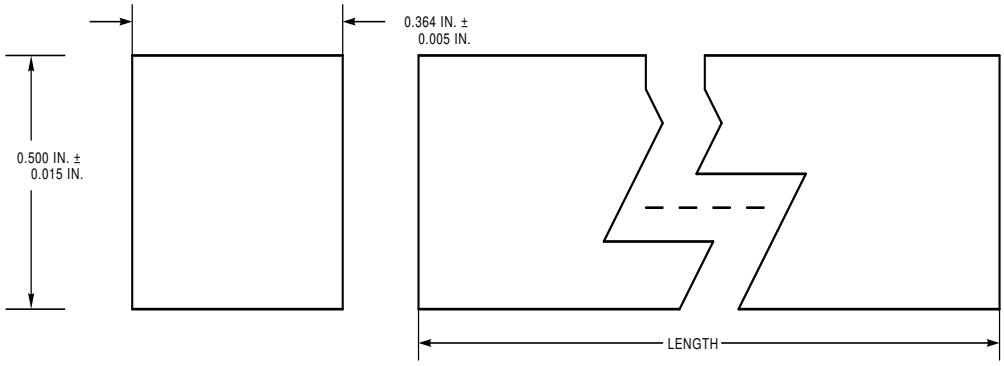
Use of available mounting bars and backplane-to-equipment configurations depend upon connector arrangement configurations. Consultation with Pre-Design Producibility is required before the correct structural support can be recommended. Mounting bars are used to support and locate wave soldered 288- and 72-pin connector blocks.

NOTE

If mounting bars are used, ensure that inner layer copper is relieved around bar mounting holes in the board.

Exhibit 2 identifies standard design data for mounting bars. Length and hole-placement dimensions are unique to each design.

Exhibit 2: Standard Design Data for Mounting Bars



MATERIAL: ALUMINUM, TYPE 2024
FINISH: CHROMATE CONVERSION COATING PER DEC 92–0020 (0–00)
COST: APPROXIMATELY $8–$10.00, FINISHED, PER 12–INCH LENGTH

RULE 7090: SUPPORT HARDWARE COSTS

Castings are preferred over mounting bars whenever possible due to lower cost and better stability.

RULE 7110: EXTERNAL CONNECTORS

External connectors, such as Berg connectors or Mate-N-Lok connectors, are allowed on sides 1 and 2. However, if mounted on side 2, they must be hand soldered after wave soldering. This adds cost, handling, and assembly time to the product.

RULE 7120: FAST-ON TABS

Fast-on tabs are not recommended due to increased assembly costs resulting from solder buildup and cut wires during wirewrap. Contact Pre-Design Producibility for alternatives.

RULE 7130: BACKPLANE DEPTH

Be sensitive to the height of the assembled backplane as there is a limit on the height that test equipment can accommodate. Contact Kanata Producibility if the height of the assembled backplane prior to test is greater than 6 inches at any point.

4 TEST RULES FOR BACKPLANES

See DEC STD 030-4, Rule 4290, for bare-board test requirements.

RULE 7140: AUTOMATIC TESTING

Backplanes shall be designed for automatic testing.

a. Preferred:

The Backplane Automated Test Systems (BATS I and BATS II) are the preferred testers for backplanes. The BATS testers test from either side of the backplane. Existing master test heads can test products using a 0.125-inch staggered grid pattern or a 0.100-inch in-line grid pattern. A standard interface head is also available to test 0.125-inch in-line grid products. Note that grid patterns cannot be intermixed on any one product for BATS testing. These testers will test for continuity on boards up to 18 by 24 inches in size. These testers are currently wired for 12,288 test points.

BATS I has been enhanced with an additional fixture to permit dual-sided testing of connectors or headers. This fixture allows 10,080 points on the top side and 2,000 points on the bottom side.

b. Not recommended for new designs:

The Automatic Wires Tester (AWT) is not recommended for new designs. The AWT tests the backplane from the module connector side using paddle cards, dual 18 fingers on 0.5-inch centers. This tester is used to test traditional wave-soldered backplanes having 288-pin or 72-pin green blocks on a 0.125-inch staggered grid.

RULE 7150: REQUIRED DATA BASE TRANSFER FOR BATS TESTING

Accurate information is required to design software and mechanical features for the Kanata tester. The following are the recommended ways to supply the required information.

a. A plot file of the UA and/or MD drawings for the product. The file should give the position and dimension of every entity on the backpanel so that the file can be regenerated on the Kanata Unigraphics system. A sample of the backplane should also be available for verification purposes.

b. Manufacturing Data Base (MDB) or ADS files giving the exact location of every test point on the backplane relative to H-Master 0. A sample of the product should also be supplied.

For additional information contact Kanata Software Engineering, DTN: 621-2270. The file must be copied directly to node KAOM06:: over DECnet since magtapes are copied with different utilities and formats.

c. Board drill listing and a sample of the product or an assembly drawing.

d. A data file is the normal prerequisite for generating BATS software. The data file should be copied directly to node KAOM06:: through DECnet. Contact Jim Keenan on POLAR::KEENAN for details.

If a data file cannot be supplied, contact Kanata Producibility. Software can be generated in other ways, such as *self-learning*, a test package on BATS using a sample product; however, this type of approach is not recommended since the software generated is only as good as the sample supplied.

NOTE

Due to the cost involved, work will not commence on volume test fixtures until the product design is formally frozen. The lead time for test fixtures is eight to ten weeks. Prototype test fixtures can be turned around in a shorter time frame if required.

e. A control drawing showing dimensions and locations of all components.

RULE 7160: WIREWRAP DATA BASE REQUIREMENTS

A wirewrap data base must be created describing all interconnection information, whether or not those connections are made by wirewrap. The wirewrap data base is required both for wiring and test purposes.

RULE 7170: LEAD PROTRUSION

The minimum lead protrusion required to support the testing of backplanes is 0.100 inch.

NOTE

Test fixturing costs may be reduced by specifying components with equal lead protrusions when mounted.

RULE 7180: PIN ACCESS FOR TEST

Pins must be accessible from side 2.

5 WIREWRAP RULES FOR BACKPLANES

RULE 7190: DESIGN USE OF WIREWRAP

Wirewrap is not recommended to be used as a design implementation. The initial design should be done solely in etch, with wirewrap being reserved for ECO activity.

RULE 7200: MAXIMUM WIREWRAP AREA

The maximum panel sizes that can be wrapped are determined by the wirewrapping machine. See Exhibit 3.

Exhibit 3: Maximum Wirewrap Area

Machine	Maximum Wrap Area (inches)
Gardner Denver (vertical)	22 x 22
N.C. semiautomatic (short)	25 x 26
N.C. semiautomatic (long)	25 x 42

RULE 7210: PIN SPACING

Backplanes that have pin spacing on a 0.100-inch by 0.100-inch square grid, 0.125-inch by 0.125-inch square grid, or 0.125-inch staggered grid spacing can be wrapped using either the Gardner Denver or N.C. semiautomatic machines. Use of mixed-grid pin spacing (for example, a mix of 0.100-inch and 0.125-inch grid spacing on one backplane) is allowed; however, Kanata Producibility should be contacted to determine software and test implications.

RULE 7220: PIN LENGTH

A minimum pin length of 0.100 inch above the board surface is required for one level of 30-gauge wirewrap. The preferred length is 0.125 inch. A minimum pin length of 0.437 inch above the board surface is required for three levels of 30-gauge wirewrap.

To ensure the stated minimum pin length for three levels of 0.437 inch wirewrap, lift-off and skewing of the circuit board above the connector blocks must not exceed 0.125 inch. Nominal lift-off is 0.031 inch.

RULE 7240: LEVELS OF WIREWRAP

The third level of wirewrap should not be used for attaching wires during initial design. This level is reserved for ECO applications and for ground pins associated with twisted-pair wires.

RULE 7250: TWISTED-PAIR WIREWRAP

- **Wirewrap** — Gardner Denver wirewrap machines cannot attach twisted pairs. Twisted pairs must be wrapped on the N.C. semiautomatic equipment.
- **Ground Pin Selection** — The optimum method for selection of pins to attach ground wires for twisted pairs involves using data available from CAD software designed to make the selection. It also involves providing soft tools for the N.C. equipment from the data. Current criteria allow a designer to have approximately 1-inch leeway on selection of a ground pin near the signal connection.
- **Routing** — Software cannot define nonstandard wire length or specify routing of twisted pairs on N.C. machines. Artwork that defines the routing path must be given to Manufacturing. A screened routing on the backplane is preferred.
- **Placement** — Twisted pairs will preferably be attached after 30 gauge discrete wirewrap connections have been made.

6 SPECIFIC RULES FOR WAVE-SOLDERED BACKPLANES

RULE 7260: THICKNESS

Maximum board thickness should not exceed 0.100 inch, as this has a major impact on the solderability of the backpanel. If a thicker backpanel is required, a press-pin alternative should be considered. Contact Kanata Producibility.

RULE 7270: THERMAL IMPEDANCE PADS

Thermal impedance pads are required on all power/ground inner layer connectors. Refer to DEC STD 030-4, Rule 4600 and DEC STD 030-4, Exhibit 18, for configuration of heat relief pads on plated-through holes up to 0.055-inch diameter. For holes larger than 0.055 inch, refer to DEC STD 030-4, Rule 4610.

RULE 7280: LARGE COPPER PLANE RELIEF

Outer layer copper planes with an area larger than 2 inches by 2 inches must be relieved. This will minimize blistering during the wave solder process.

RULE 7290: LINE WIDTH AND SPACING

See DEC STD 030-4, heading 3.6 for line width and spacing requirements.

For other general rules on conductor spacing and routings, refer to DEC STD 030-5, Rule 5195 through DEC STD 030-4, Rule 4460.

RULE 7300: STANDARD GRID

The standard configuration for green block layout shall be 0.125 inch staggered grid relative to H-Master 0. For other rules governing standard grids, refer to DEC STD 030-4, Exhibit 4 and DEC STD 030-4, Exhibit 5.

RULE 7310: PLATED-THROUGH HOLES

The finished plated-through hole size for the 0.025-inch square pin on the 288-pin, 72-pin, or 36-pin connector block is 0.042 inch ± 0.005 inch diameter. The full range of hole sizes and tolerances is given in *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*.

RULE 7320: SIDE 2 COMPONENTS

Avoid placing components on side 2 when possible. The additional handling for the hand solder operation can cause quality problems resulting in a greater number of rejects and high product cost.

RULE 7330: HOLD-DOWN MOUNTING HOLES

Drilled holes with a 0.187-inch diameter are required for fixturing to hold the board down during wave soldering. One hole is required for every two 288-pin connector blocks. Holes are mandatory for all multilayer backpanels and for all double-sided panels over nine slots wide. Ensure that inner plane copper is relieved around these holes.

RULE 7340: ASSEMBLY FEATURES

Standard assembly fixturing is available for up to 48 slots on 0.500-inch module-to-module centers. Pre-Design Producibility should be consulted to determine if proposed design configurations can be outfitted with standard fixturing. Other fixtures will be designed to product requirements.

RULE 7350: EDGE CLEARANCE

Component bodies or hardware shall not be placed within 0.200 inch of any edge of the backpanel. This will make it possible to attach plows and other support hardware for the wave-solder process.

RULE 7380: CONNECTORS

There are three standard connector blocks that provide for module interconnection and contain 0.025-inch square wire-wrappable posts on a 0.0125-inch staggered grid:

288-pin	Part number 12-10258-01
72-pin	Part number 12-11425-00
36-pin	Part number 12-11029-00

7 SPECIFIC RULES FOR PRESS-PIN BACKPLANES

Contact Kanata Producibility with any problems concerning Rule 7390 through Rule 7450.

RULE 7390: BOARD THICKNESS

The preferred board thickness is 0.125 ± 0.015 inch. Contact Pre-Design Producibility if a different board thickness must be used. The minimum allowable board thickness for a press-pin backplane is 0.093 inch.

RULE 7410: STANDARD GRID

The standard configuration for press-pin layout shall be 0.100 inch by 0.100 inch or 0.125 inch by 0.125 inch, in-line fixed grid relative to H-Master 0. For other rules governing standard grids, refer to DEC STD 030-4, Exhibit 4 and DEC STD 030-4, Exhibit 5.

RULE 7420: PLATED-THROUGH HOLES

The finished plated-through hole size for a press-pin hole must be maintained at 0.041 inch +0.002/-0.003 inch. Board drawings for press-pin backpanels must specify this hole size and tolerance. For other than press-pin hole sizes, refer to *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*.

RULE 7430: PAD SIZE

The minimum pad size for the 0.041-inch square press-pin hole shall be 0.060 inch on both sides.

RULE 7440: TOOLING HOLES

A minimum of two diagonally-opposed tooling holes are required. Four are preferred and may be necessary for the surface mount process. These should be located at 0.200-inch offsets close to each corner of the board. The diameter of each tooling hole should be as stated in *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria* with no pad or plating.

Refer to DEC STD 030-4, Exhibit 17, for inner layer clearance requirements for plated-through holes. General requirements for PWB markings are covered in DEC STD 030-4, Exhibit 2.

RULE 7450: COMPONENT CLEARANCE REQUIREMENTS AROUND TOOLING HOLES

As a minimum, the area within a radius of 0.200 inch around backplane tooling holes shall be free of components to ensure that the backplane will seat properly on press-pin and test fixtures. If it is not possible to maintain this clearance, contact Kanata Producibility.

RULE 7460: STANDARD PRESS-PIN CONNECTORS

The standard press-pin connectors available at this time are:

- **Dual 47** - 94 pin on 0.100-inch by 0.100-inch centers

  12-18421-02 - Gold-plated tails
  12-18421-03 - Tin/lead-plated tails
  12-18421-05 - Tin/lead-plated short tails

- **Dual 37** - 74 pin on 0.100-inch by 0.100-inch centers

  12-18421-04 - Tin/lead-plated short tails

- **Dual 36** - 72 pin on 0.125-inch by 0.125-inch centers

  12-18422-00 - Gold tails, unslotted ends
  12-18422-01 - Tin/lead tails, unslotted ends
  12-18422-04 - Gold tails, slotted ends
  12-18422-05 - Tin/lead tails, slotted ends

- **Dual 18** - 36 pin on 0.125-inch by 0.125-inch centers

  12-18422-06 - Gold tails, unslotted ends
  12-18422-07 - Tin/lead tails, unslotted ends

Refer to A-PS-1400000-GS-0, *Connector Assemblies, Card-Edge Type, Press Pin, General Specification for*, for specifications regarding all press-pin components.

RULE 7470: MODULE THICKNESS

The 0.125-inch by 0.125-inch and 0.100-inch by 0.100-inch in-line press-pin connector require a plug-in module thickness of 0.054 to 0.068 inch.

The BATS test system is designed to test backplanes with pins on a 0.125-inch staggered grid. For 0.100-inch grid or mixed grid, an interface head, which mates the 0.125-inch staggered machine grid to the grid of the press pin backplane, must be designed and built. A board drill tape and artwork of the circuit must be supplied in order to fabricate the template.

RULE 7480: PRESS-PIN COMPONENT CLEARANCE

There shall be a 0.100-inch clearance between press-pin connectors and any other components to allow for repair and removal tools.

8 SPECIFIC DESIGN AND ASSEMBLY RULES FOR BACKPLANES WITH SURFACE-CONTACT CONNECTORS

The alignment of the backplane to the cardcage is critical. Usually the two parts cannot be separated as distinct field replaceable units (FRU).

RULE 7500: SURFACE CONNECTORS AND SOLDERING

Do not use surface pressure contact connectors with through hole soldering.

RULE 7510: HOLD-DOWN HARDWARE

The hold-down hardware and torquing/inspection criteria must be explicitly defined to avoid connector relaxation.

RULE 7520: SURFACE-CONTACT CONNECTOR PAD HEIGHTS

Refer to *DEC STD 176-0 Printed-Wiring Board Acceptance Criteria* for pad heights for pressure contact.

RULE 7530: BOARD SURFACE FINISH

Backplane boards with surface pressure contact pads shall not be specified as SMOBC.

9 SPECIFIC DESIGN RULES FOR BACKPLANES WITH SURFACE MOUNT COMPONENTS

See DEC STD 030-5 for general SMT assembly rules.

Kanata requires product information, hard and soft tools, and product kits to start up a new backplane in a surface mount assembly area. Contact Kanata engineering for the full list of requirements.

RULE 7550: KANATA SMT PROCESS CONSTRAINTS

The following are Kanata process constraints for SMT backplanes

- SMT components, tooling holes, and fiducials shall be placed within a 16-inch x 18-inch onsertion window.
- The maximum board size shall be 16-inch x 24-inch x ¼-inch thick.

Contact Kanata Engineering for the impact of a design exceeding these constraints.

REFERENCED DOCUMENTS

EL-Class Digital Documents

EL-Class Number	Document Title
EL-00016-00	*DEC STD 016-0 Printed-Wiring Board and Module Manufacturing Terminology*
EL-00030-01	*DEC STD 030-1 Module Manufacturing Standard - General Producibility Requirements*
EL-00030-02	*DEC STD 030-2 Module Manufacturing Standard - Product Safety Requirements*
EL-00030-04	*DEC STD 030-4 Module Manufacturing Standard - Printed-Wiring Board Design Requirements*
EL-00030-05	*DEC STD 030-5 Module Manufacturing Standard - Module Assembly Rules*
EL-00176-00	*DEC STD 176-0 Printed-Wiring Board Acceptance Criteria*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

Other Documents

Document Number	Document Title
A-PS-1400000-GS-0	*Connector Assemblies, Card-Edge Type, Press Pin, General Specification for*

Purchase Specifications are available from any Microfilm Reference File (35mm aperture card "tub") or the SPOC system.

DEC STD 030-7 RULES INDEX

Rule 7000: Finished Board Size, 2
Rule 7010: Backpanel Shearing/Routing, 2
Rule 7020: Base Laminate Material, 3
Rule 7030: Soldermask, 3
Rule 7040: Copper Inner Layer Thickness, 3
Rule 7050: Preferred Inner Layer Clearance Pad Sizes, 3
Rule 7060: Backpanel Nomenclature, 3
Rule 7070: Standard Castings, 4
Rule 7080: Mounting Bars and Backplane-To-Equipment Configurations, 4
Rule 7090: Support Hardware Costs, 5
Rule 7110: External Connectors, 5
Rule 7120: Fast-On Tabs, 5
Rule 7130: Backplane Depth, 5
Rule 7140: Automatic Testing, 6
Rule 7150: Required Data Base Transfer for BATS Testing, 6
Rule 7160: Wirewrap Data Base Requirements, 6
Rule 7170: Lead Protrusion, 6
Rule 7180: Pin Access for Test, 6
Rule 7190: Design Use of Wirewrap, 7
Rule 7200: Maximum Wirewrap Area, 7
Rule 7210: Pin Spacing, 7
Rule 7220: Pin Length, 7
Rule 7240: Levels of Wirewrap, 8
Rule 7250: Twisted-Pair Wirewrap, 8
Rule 7260: Thickness, 8
Rule 7270: Thermal Impedance Pads, 8
Rule 7280: Large Copper Plane Relief, 8
Rule 7290: Line Width and Spacing, 8
Rule 7300: Standard Grid, 9
Rule 7310: Plated-Through Holes, 9
Rule 7320: Side 2 Components, 9
Rule 7330: Hold-Down Mounting Holes, 9
Rule 7340: Assembly Features, 9
Rule 7350: Edge Clearance, 9
Rule 7380: Connectors, 9
Rule 7390: Board Thickness, 10
Rule 7410: Standard Grid, 10
Rule 7420: Plated-Through Holes, 10
Rule 7430: Pad Size, 10
Rule 7440: Tooling Holes, 10
Rule 7450: Component Clearance Requirements Around Tooling Holes, 11
Rule 7460: Standard Press-Pin Connectors, 11

Rule 7470: Module Thickness, 11
Rule 7480: Press-Pin Component Clearance, 11
Rule 7500: Surface Connectors and Soldering, 12
Rule 7510: Hold-Down Hardware, 12
Rule 7520: Surface-Contact Connector Pad Heights, 12
Rule 7530: Board Surface Finish, 12
Rule 7550: Kanata SMT Process Constraints, 12

INDEX

A

ADS Files, 6
Aqueous Cleaner, Backpanel Sizes, 2
Artwork
  Layout, Backpanel, 3
  Routing Path, 8
Assembly
  Fixturing, 9
  Rules for Backplanes, 4
Automatic
  Testing, Backplane, 5

B

Backpanel
  Nomenclature, 3
  Shearing/Routing, 2
  Sizes, 2
  Solderability, 8
Backpanel Automated Test Systems (BATS), 2, 5, 11
Backplane
  Assembly Rules, 4
  Design Rules, 2
  Press-Pin, 10
  Producibility, 2
  Test Rules, 5
  Wave-Soldered, 8
Backplane-To-Equipment Configurations, 4
Base
  Laminate Material, 3
BATS Test
  See Backpanel Automated Test Systems
Berg Connectors, 5
Board
  Drill Listing, 6
  Thickness, Press-Pin Backplane, 10
Bonding Sheets, 3
Bussed and Wired Backplane, 1

C

Castings, 4
Clearance
  Inner Layer, Pad Sizes, 3
Component
  Clearance Around Tooling Holes, 11
Component (Cont.)
  Nomenclature Locations, 3
Connector
  Berg, 5
  Blocks, 9
  External, 5
  Mate-N-Lok, 5
  Surface-Contact, 2, 12
Copper
  Inner Layer Thickness, 3
  Plane Relief, 8

D

Data Base Transfer, BATS Testing, 6
Depth, Backplane, 5
Design
  Data, Mounting Bars, 4
  Rules, Backplane, 2
  Use of Wirewrap, 7
Double-Sided
  PTH, 1
Drill Tape, 11

E

ECO
  Applications, 8
Edge Clearance, Backplane, 9
External
  Connectors, 5

F

Fast-On Tabs, 5
Fine Line Technology
  Backplane, 3
Finished
  Board Size, Backpanels, 2
FR-4
  Laminates, 3

G

Ground
  Pin Selection, 8
GSO Process, Backpanels, 2

H

Heat Relief Pads, 8
Height, Backplane, 5
Hex
  Module Castings, 4
High Density Technology, 3
Hold-Down Mounting Holes, 9

I

Impedance
  Pads, Thermal, 8
Inner Layer
  Clearance, 3
  Copper, 4
  Thickness, Copper, 3

L

Lead
  Protrusion, 6
LIF
  See Low Insertion Force Connector
Liftoff, Wirewrap, 7
Low Insertion Force Connector (LIF), 2

M

Manufacturing
  Data Base, 6
  Technologies, 2
Mate-N-Lok Connectors, 5
Mixed
  Grid Pin Spacing, 7
  Technology Designs, 2
Module
  Drawings, 2, 6
  Thickness, Backplane, 11
Mounting
  Bars, 4
  Holes, 9
Multilayer
  Backplane, 1
Multisignal Layer (MSL)
  Backplane, 1
  Pads-Only Boards, 3

N

Nomenclature
  Backpanel, 3
Nominal
  Liftoff, Wirewrap, 7
Nonstandard
  Wire Length, 8

P

Pad
  Size, 3, 10
Pin
  Access for Test, 6
  Spacing and Length, 7
Plated-Through Holes (PTH), 9, 10
Power/Ground Inner Layer Connectors, 8
Pre-Design
  Producibility, 2
Pre-Preg, 3
Press-Pin
  Backplanes, 10
  Connectors, 11
  Machine, Backpanels, 2
Producibility
  Backplane, 2
Prototype Test Fixtures, 6

R

Routing
  Backpanels, 2
  Twisted Pairs, 8

S

Screened
  Nomenclature, 3
  Routing, 8
Shearing
  Backpanels, 2
Side 2 Components, 9
Single
  Sided PC Board, 1
Solderability
  Board Thickness, 8
  Nomenclature, 3
Soldered
  Backpanel, 3
Soldermask
  Backpanel, 3
Soldermask Over Bare Copper (SMOBC), 3
Spacing
  Backplanes, 8
Standard
  Castings, 4
  Connector Blocks, 9
  Grid, Press-Pin Backplane, 10
  Grid, Wave-Soldered Backplane, 9
Support Hardware Costs, 5
Surface
  Contact Connectors, 2, 12
Surface Mount
  Test, Backpanels, 2

T

Test
  Points, 6
  Rules for Backplanes, 5
Thermal Impedance Pad, 8
Thickness
  Press-Pin Backplane, 10
  Wave-Soldered Backplane, 8
Tooling
  Hole, 10, 11
Twisted-Pair Wirewrap, 8

U

UA Drawings, 6

V

Volume
  Test Fixtures, 6

W

Wave Solder
  Backplane Rules, 8
  Machine, Backpanels, 2
Wirewrap
  Data Base Requirements, 6
  Rules, Backplane, 7

Z

Zero Insertion Force Connector (ZIF), 2

```
+---------------------------------------------------------------------+
|                        READER COMMENTS                              |
|                                                                     |
| Your  comments  and suggestions  will help  Standards and Methods   |
| Control improve their services and documents.                       |
+---------------------------------------------------------------------+
```

Did you request this document? _____ If so, did it arrive within a satisfactory period of time? _____ Please comment.

What are your impressions of this document? Consider format, organization, completeness, readability, and illustrations.

————————**FOLD ON THIS LINE**————————————————————————

Did you find technical or clerical errors in this document? If so, please specify the page number(s) and the error(s).

Are the instructions for the update package clear? _____
Was an index available? _____ If not, is one needed? _____
Do you have other suggestions for improving this document?

The following information is optional:

Name _____ Mailstop _____

Department _____ Node _____

Send your comments to JOKUR::PROJECTS, or fold, staple, and send this page through interoffice mail to:

```
+-------------------------------+
|       READERS' COMMENTS       |
| STANDARDS AND METHODS CONTROL |
|           NRO4/D4             |
+-------------------------------+
```